

CS 47

Midterm 2 Study Hints

Topics

- Procedures
- Arrays
- Structures
- Y86 instruction set
- Logic design
- SEQ Processor

class19.ppt

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Procedures

Assembly code for

Passing arguments

Stack management

Call / Return

Section 3.7, Practice Problems 3.14, 3.15, 3.16

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Arrays

Assembly code for

Accessing elements with subscripts

Accessing elements with pointers

Nested arrays, two dimensional arrays

Section 3.8, Practice Problems 3.17, 3.18, 3.19, 3.20

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Structures and Unions

C and Assembly code for

Computing offsets

Accessing elements

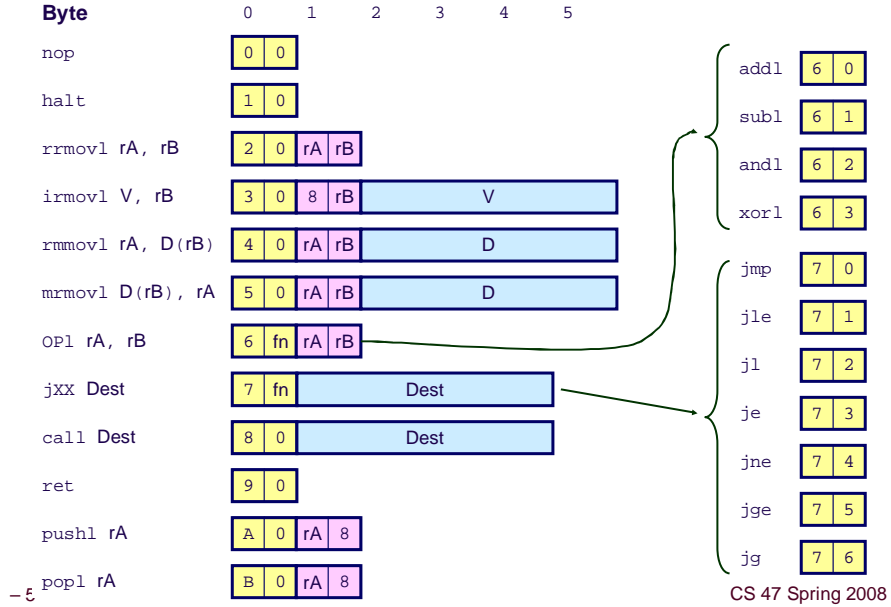
Nested structures, unions

Section 3.9, Practice Problems 3.21, 3.22

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Y86 Instruction Set



Y86 Registers

Number	Register	Number	Register
0	%eax	4	%esp
1	%ecx	5	%ebp
2	%edx	6	%esi
3	%ebx	7	%edi
		8	No register

Y86 Instruction Set

Converting assembly code to machine code (Prob. 4.1)

Converting machine code to assembly code (Prob. 4.2)

Converting IA32 code to Y86 (Prob. 4.3)

Section 4.1

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Y86 Instruction Set

Converting assembly code to machine code (Prob. 4.1)

Converting machine code to assembly code (Prob. 4.2)

Converting IA32 code to Y86 (Prob. 4.3)

Section 4.1

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Logic Design and HCL

Gates: And, Or, Not

HCL Boolean expressions (Prob. 4.6)

HCL integer expressions (Prob. 4.7, 4.8)

Memory, registers, and clocking

Section 4.2

SEQ Stages

Fetch

- Read instruction from instruction memory

Decode

- Read program registers

Execute

- Compute value or address

Memory

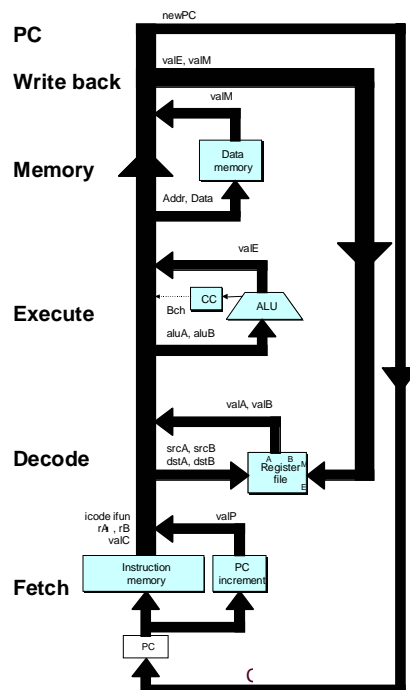
- Read or write data

Write Back

- Write program registers

PC

- Update program counter



SEQ Processor Design

Six stages

Tracing the stages for various instructions (Prob. 4.9, 4.10)

Use of processor resources by instructions

e.g., why is there no register-to-memory add?

In less detail:

Effects of modifying instructions or processor (Prob. 4.11 – 4.13)

Designing the control logic (Prob. 4.14 – 4.20)

Subsections 4.3.1 – 4.3.4