San Jose State University
CS 286: Special Topics in Advanced Parallel Processing
Fall 2010 Course Syllabus

Description: A combination hardware architecture and software development class focused on multi-threaded, parallel processing algorithms and techniques. Overview of high-performance parallel processing hardware architectures ranging from on-chip Instruction-Level Parallelism to multi-core microprocessor chips to large distributed supercomputing systems including Clusters, Grids, and Clouds. Discussion and hands-on exercises in a broad range of various parallel programming paradigms and languages such as MPI, OpenMP, Map-Reduce Hadoop, CUDA and OpenCL. The class focus will be on understanding the fundamental concepts associated with the design and analysis of parallel processing systems. Special emphasis will be placed on avoiding the unique non-deterministic software defects that can arise in parallel processing systems including race conditions and deadlocks. The class will also provide an overview of current parallel software development toolkits including debuggers and performance profilers. A special feature of this Fall 2010 class is that students will have the opportunity to use two pilot systems: A Cloud Development Platform from IBM, and A Multi-Core Testing Lab from Intel.

Meeting Time: Section 1: MW 1500-1615 MH422

Prerequisites: CS 159 or equivalent, or instructor consent.

Instructor: Robert K. Chun

Contact Info: EMAIL: ProfessorChun@gmail.com, PHONE: (408) 924-5137, OFFICE: MH 413

Office Hours: MW 16:15 – 17:45


Grading: Grading consists of two midterms, one final, and a set of projects consisting of a combination of written problems and programming assignments. All assignments must be completed by the student on the due date specified to receive credit for the class. Late assignments or exams are not accepted. All students must uphold academic integrity as detailed at http://www2.sjsu.edu/senate/f88-10.htm

Student Learning Outcomes:

Upon successful completion of this course, students will be able to understand how to design and develop parallel programs that can effectively leverage the new multi-core chip and Cloud technologies being built by industry.